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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SERRAO, RANODHI N	

ART UNIT	PAPER NUMBER
2141	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,529	PESHKIN ET AL.	
	Examiner	Art Unit	
	Ranodhi Serrao	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30,32-35,37-44,55,59 and 60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30,32-35,37-44,55,59 and 60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 27 October 2005 have been fully considered but they are not persuasive. Applicant's arguments with respect to amended claims 1, 29, 32-35, 37-39, and 55 and to the newly added claims 59 and 60 have been addressed in the rejections below.

2. Furthermore the applicant argued that Johnson does not teach a broadcast-packet-processing device. The examiner points to col. 53, lines 16-48, wherein Johnson shows DSP 78 which functions as a broadcast-packet-processing device.

3. The applicant also argued that O'Toole does not mention determination of whether "boot-control code has previously been executed." The examiner points to col. 11, line 63-col. 12, line 13 wherein O'Toole teaches the claimed limitation.

4. Moreover, the applicant argued that Walker fails to disclose directing a device to enter a process-initial-address-assignment mode and an ignore-initial-address-assignment mode. The examiner reaffirms the previous rejections for the claimed limitations.

5. The applicant argued that Krause teaches devices that are hardwired to have two (or more) specific addresses during manufacture. The examiner points to col. 7, line 54-col. 8, line-6, wherein Krause shows addresses that are not hardwired.

6. The applicant argued that Baker does not teach a "multi-channel device, having a Slave Initial Boot Packet Processing Device." The examiner points to col. 12, lines 44-62. This paragraph clearly teaches the invention as claimed.

7. The examiner reaffirms the combination of Baker in view of Brooks since the motivation to combine resides in Brooks, see paragraph 39. In conclusion, the prior arts of record teach the invention as claimed.

Claim Rejections - 35 USC § 102

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson (6,366,578) and Walker et al. (5,862,338).

10. As per claim 1, Johnson teaches a system comprising: a broadcast-capable switch (col. 53, lines 16-48); a host processor operably coupled with the broadcast-capable switch (column 10, line 63-column 11, line 18); a first broadcast-packet-processing device operably coupled with the broadcast-capable switch (column 11, lines 19-27); a second broadcast-packet-processing device operably coupled with the broadcast-capable switch (column 11, lines 28-37); and at least one of the first broadcast-packet-processing device and the second broadcast-packet-processing device operably coupled with the host processor (column 12, lines 35-61), the host processor being configured to selectively transmit an attend signal to the at least one of the first broadcast-packet-processing device and the second broadcast-packet-processing device to which is operably coupled (col. 8, line 55-col. 9, line 10: wherein enabling automatic internal negotiation serves the function of an attend signal).

11. As per claim 2, Johnson teaches a system wherein said at least one of the first broadcast-packet-processing device and the second broadcast-packet-processing device operably coupled with the host processor comprises: the first broadcast-packet-processing device and the second broadcast-packet-processing device operably coupled with the host processor (column 12, lines 35-61).

12. As per claim 3, Johnson teaches a system wherein said at least one of the first broadcast-packet-processing device and the second broadcast-packet-processing device operably coupled with the host processor comprises: the first broadcast-packet-processing device operably coupled with the host processor (column 11, lines 28-37); and the second broadcast-packet-processing device operably coupled with the first broadcast-packet-processing device (column 10, line 63-column 11, line 18).

13. As per claim 4, Johnson teaches a system wherein said broadcast-capable switch comprises: an Ethernet-capable switch (column 15, lines 28-49).

14. As per claim 5, Johnson teaches a system wherein said Ethernet-capable switch comprises: a shared medium Ethernet switch (column 12, line 62-column 13, line 6).

15. As per claim 6, Johnson teaches a system wherein said Ethernet-capable switch comprises: a non-shared medium Ethernet switch (column 9, line 63-column 10, line 20).

16. As per claims 7 and 9, Johnson teaches an Ethernet-broadcast-packet-processing device and an Ethernet-capable switch operable coupled by a shared medium (column 11, line 41-column 12, line 23 and column 3, lines 18-41).

17. As per claims 8 and 10, Johnson teaches an Ethernet-broadcast-packet-processing device and an Ethernet-capable switch operably coupled by a non-shared medium (column 11, line 41-column 12, line 23 and column 3, lines 18-41).

18. As per claim 11, Johnson teaches a system wherein said first broadcast-packet-processing device comprises: an address-assignment-recognition device (column 7, lines 21-47).

19. As per claim 12, Johnson teaches a system wherein said second broadcast-packet-processing device comprises: an address-assignment-recognition device (column 7, lines 21-47).

20. Claims 55, 59, and 60 are rejected under 35 U.S.C. 102(e) as being anticipated by O'Toole et al. (6,345,294).

21. As per claim 55, O'Toole et al. teaches a system and a method comprising: receiving a broadcast packet having an initial boot-up message comprises: determining that boot-control code has previously been executed; and sending an acknowledgment (column 12, lines 42-64).

22. As per claim 59, O'Toole et al. teaches a method of booting a computing device, the method comprising: receiving a broadcast packet having an initial boot message (col. 7, lines 36-60); when a boot-control code has not previously been executed by the computing device (col. 12, lines 42-64): executing the boot control code in response to the received broadcast packet (col. 11, lines 8-25); and sending an acknowledgement (col. 12, lines 14-21); and when the boot-control code has previously been executed by

the computing device, sending an acknowledgement in response to the received broadcast packet (col. 12, lines 42-64).

23. As per claim 60, O'Toole et al. teaches a method wherein the computing device comprises a broadcast-packet processing device (col. 8, lines 17-34).

24. Claims 13-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Walker et al. (5,862,338).

25. As per claims 13 and 21, Walker et al. teaches a method comprising: directing at least one of a first broadcast-packet-processing device and a second broadcast-packet-processing device to enter an ignore-initial-address-assignment mode (column 6, line 52-column 7, line 10); directing the first broadcast-packet-processing device to enter a process-initial-address-assignment mode (column 50, lines 15-37); transmitting a broadcast packet containing payload having an address-assignment message intended for the first broadcast-packet-processing device (column 55, lines 26-36); directing the second broadcast-packet-processing device to enter a process-initial-address-assignment mode (column 8, line 59-column 9, line 24); and transmitting a broadcast packet containing payload having an address-assignment message intended for the second broadcast-packet-processing device (column 55, lines 37-61).

26. As per claims 14 and 22, Walker et al. teaches a method wherein said directing a first broadcast-packet-processing device and a second broadcast-packet-processing device to enter an ignore-initial-address-assignment mode comprises: forcing a first attend-ignore line associated with the first broadcast-packet-processing device into an

ignore value (column 57, lines 1-17); and forcing, substantially simultaneously with said forcing the first attend-ignore line, a second attend-ignore line associated with the second broadcast-packet-processing device into an ignore value (column 26, lines 36-60).

27. As per claims 15 and 23, Walker et al. teaches a method, wherein said directing a first broadcast-packet-processing device and a second broadcast-packet-processing device to enter an ignore-initial-address-assignment mode comprises: forcing a first attend-ignore line associated with the first broadcast-packet-processing device into an ignore value (column 57, lines 1-17); and forcing, sequential to said forcing the first attend-ignore line, a second attend-ignore line associated with the second broadcast-packet-processing device into an ignore value (column 53, lines 1-23).

28. As per claims 16 and 24, Walker et al. teaches a method, wherein said directing the first broadcast-packet-processing device to enter a process-initial-address-assignment mode comprises: forcing a first attend-ignore line associated with the first broadcast-packet-processing device into an attend value (column 13, lines 11-26).

29. As per claims 17 and 25, Walker et al. teaches a method, wherein said directing the second broadcast-packet-processing device to enter a process-initial-address-assignment mode comprises: forcing a second attend-ignore line associated with the second broadcast-packet-processing device into an attend value (column 13, lines 34-55).

30. As per claims 18 and 26, Walker et al. teaches a method, wherein said forcing a second attend-ignore line associated with the second broadcast-packet-processing

device into an attend value comprises: the first broadcast-packet-processing device forcing the second attend-ignore line associated with the second broadcast-packet-processing device into the attend value (column 11, lines 14-39).

31. As per claims 19 and 27, Walker et al. teaches a method, wherein said transmitting a broadcast packet containing payload having an address-assignment message intended for the first broadcast-packet-processing device comprises: transmitting a broadcast packet containing payload having an address-assignment message intended for the first broadcast-packet-processing device until an acknowledgment from the first broadcast-packet-processing device is received (column 20, lines 24-44).

32. As per claims 20 and 28, Walker et al. teaches a method, wherein said transmitting a broadcast packet containing payload having an address-assignment message intended for the second broadcast-packet-processing device comprises: transmitting a broadcast packet containing payload having an address-assignment message intended for the second broadcast-packet-processing device until an acknowledgment from the second broadcast-packet-processing device is received (column 21, lines 10-32).

33. Claims 29-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Krause et al. (5,590,285).

34. As per claims 29 and 34, Krause et al. teaches a method comprising: receiving a broadcast packet containing payload having an specific-address assignment message

(column 2, lines 50-56); accepting an address assignment as indicated by the specific-address assignment message (col. 7, line 66-col. 8, line 6); and sending an acknowledgement upon completion of said accepting the address assignment as indicated by the specific-address assignment message (co. 2, line 57-col. 3, line 8).

35. As per claims 30 and 35, Krause et al. teaches a method, wherein said receiving a broadcast packet containing payload having a specific-address assignment message comprises: receiving a broadcast packet containing payload having an specific Media Access Control (MAC) address assignment message (column 2, line 57-column 3, line 8).

36. As per claims 32 and 37, Krause et al. teaches a method, further comprising: receiving a second broadcast packet containing payload having the specific-address assignment message (col. 8, lines 7-17); recognizing that an address assignment as indicated by the specific-address assignment message has already been achieved (column 11, lines 3-9); and sending an acknowledgment of the address assignment indicated by the specific-address assignment message (column 11, line 66-column 12, line 14).

37. As per claims 33 and 38, Krause et al. teaches a method, further comprising: receiving a second broadcast packet containing payload having a second specific-address assignment message (col. 8, lines 7-17); determining that an address assignment different from the specific-address has previously been accepted (column 17, lines 16-48); and ignoring the second specific-address assignment message (column 17, lines 49-60).

38. Claims 39-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Baker (6,081,852).

39. As per claim 39, Baker teaches a system comprising: a packet switch; a host processor operably coupled with the packet switch (column 6, lines 13-23 and column 29, lines 35-50); a first multi-channel device, having a Slave Initial Boot Packet Processing Device, operably coupled with the packet switch (column 7, lines 10-27); and a second multi-channel device, having a Slave Initial Boot Packet Processing Device, operably coupled with the packet switch (column 5, lines 14-25).

40. As per claim 40, Baker teaches a system, wherein said first multi-channel device is substantially indistinguishable from said second multi-channel device (figure 1, items 30 and 32).

41. As per claim 41, Baker teaches a system, wherein said first multi-channel device is substantially indistinguishable from said second multi-channel device comprises: said first multi-channel device having a first a boot-control code Read Only Memory (column 4, lines 25-44); and said second multi-channel device having a second boot-control code Read Only Memory substantially similar to the first boot-control code Read Only Memory (column 5, line 51-column 6, line 4).

Claim Rejections - 35 USC § 103

42. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

43. Claims 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker (6,081,852) as applied to claim 39 above, and further in view of Brooks et al. (2001/0039600).

44. As per claim 42, Baker teaches the mentioned limitations of claim 39 above but fails to teach a system, wherein said first multi-channel device, having a Slave Initial Boot Packet Processing Device, operably coupled with the packet switch comprises: a first packet-processing device, having an assigned address, uniquely coupled with the first multi-channel device. However, Brooks et al. teaches a system, wherein said first multi-channel device, having a Slave Initial Boot Packet Processing Device, operably coupled with the packet switch comprises: a first packet-processing device, having an assigned address, uniquely coupled with the first multi-channel device (see Brooks et al. paragraph 0031). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the system of claim 39 to a system, wherein said first multi-channel device, having a Slave Initial Boot Packet Processing Device, operably coupled with the packet switch comprises: a first packet-processing device, having an assigned address, uniquely coupled with the first multi-channel device in order to minimize system latency and data buffering for certain peripherals.

45. As per claim 43, Baker teaches the mentioned limitations of claim 39 above but fails to teach a system, wherein said second multi-channel device, having a Slave Initial Boot Packet Processing Device, operably coupled with the packet switch comprises: a second packet-processing device having an assigned address, uniquely coupled with the first multi-channel device. However, Brooks et al. teaches a system, wherein said

second multi-channel device, having a Slave Initial Boot Packet Processing Device, operably coupled with the packet switch comprises: a second packet-processing device having an assigned address, uniquely coupled with the first multi-channel device (see Brooks et al. paragraph 0035). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the system of claim 39 to a system, wherein said second multi-channel device, having a Slave Initial Boot Packet Processing Device, operably coupled with the packet switch comprises: a second packet-processing device having an assigned address, uniquely coupled with the first multi-channel device because a MAC address allows other devices in the network to locate specific ports in the network and to create and update routing tables and data structures (see Brooks et al. paragraph 0009).

46. As per claim 44, Baker teaches the mentioned limitations of claims 39 and 43 above but fails to teach a system, wherein the second packet-processing device having an assigned address comprises: the second packet-processing device having an assigned Media Access Control address. However, Brooks et al. teaches a system, wherein the second packet-processing device having an assigned address comprises: the second packet-processing device having an assigned Media Access Control address (see Brooks et al. paragraph 0035). It would have been obvious to one having ordinary skill in the art at the time of the invention to modify the systems of claims 39 and 43 to a system, wherein the second packet-processing device having an assigned address comprises: the second packet-processing device having an assigned Media Access Control address in order to allow other devices in the network to locate specific

ports in the network and to create and update routing tables and data structures (see Brooks et al. paragraph 0009).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ranodhi Serrao whose telephone number is (571)272-7967. The examiner can normally be reached on 8:00-4:30pm, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia can be reached on (571) 272-3880. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RUPAL DHARIA
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